FMEA NO. 1.2.23

CRITICALITY 2/2

SHUTTLE CCTV
CRITICAL ITEMS LIST

UNIT Video Switching Unit (VSU)
DHB NO. 2294823-502, 504

SHEET 1 OF 7

FAILURE MODE AND CAUSE	FAILURE EFFECT ON END ITEM	RATIONALE FOR ACCEPTANCE
Loss of odd-field sync signal. Cause: (1) Timing Logic, Logic Board. A3, 2294891-502 or 2592392-501	Loss of video routing capability. Worst Case: Loss of mission critical observations via CCTV system.	DESIGN FEATURES The VSU is a microprocessor-based video switching unit using an RCA 1802 microprocessor, CMOS RAM, and ITL PROM. Computer I/O, decoding logic, digital audio and switch control circuitry are implemented in CMOS CD4000 series logic to minimize power dissipation. The design incorporates DMOS FET devices (SD211s) purchased to an RCA spec control drawing (SCD) as the basic video switch element. Video split-screen capability incorporates glass delay line modules procured from Microsonics (orfginally Corning) to an RCA SCD. The video amplifier design uses monolithic NE5539 wideband op amps in a fashion similar to the sync amp design employed in the RCU. Parts were required to be JAN reliability level parts of their equivalent. Part selection falls into three categories: (1) JAN or better parts from the Military QPL, (2) Parts demonstrated to NASA to be equivalent to JAN level via test data (e.g., CD4000/3N series parts), or (3) Parts procured to an RCA spec control drawing which calls out tests and screening to effect JAN equivalency. BARE BOARD CONSTRUCTION (A3) The boards are of "welded wire" construction. At the bare board level this does not distinguish it from a normal PC board except that holes which will take weld pins generally are not connected to PC traces. Only those pins which bring power and ground potentials to the ICs are on PCs. An annular ring surrounds the hole in the board where each power and ground pin is located. These pins are then soldered to the trace like any other component lead. Aside from this feature, all design & construction techniques used in PC board layout apply. BOARD ASSEMBLY (A3) The drilled and etched boards are populated with several hundred solderable or weldable pins. Power and ground pins, as well as connector pins, are soldered in place. Discreet components (resistors, diodes, capacitors) are attached to bifurcated terminals, where they are soldered. Flatpack ICs are welded, lead-by-lead, to the tops of the weld pins. After welding, extra lead material is trimmed away. Circuit connections are made using #30 AWG nickel weld wire. The wire is welded to the pin surfaces on the board backside. All wire welds are done using a machine which is tape driven, thus eliminating the possibility of miswiring due to operator error. All wiring & circuit performance is tested prior to box-level installation. After successful testing, components are staked as required by drawing notes and the assembly is coated with urethane.

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FAILURE MODE AND CAUSE	FAILURE EFFECT ON END ITEM	RATIONALE FOR ACCEPTANCE
Loss of odd-field sync signal. Cause: (1) Timing logic, Logic Board, A3, 2294891-502 or 2592392-501	Loss of video routing capability. Worst Case: Loss of mission critical observations via CCTV system.	DESIGN FEATURES The board is inserted in the box on card-edge guides, in the same manner as the other PC boards. BOARD PLACEMENT The A3, board is secured in the electronics assembly by gold-plated beryllium copper card guides. Connections are made to the mother board with blind-mated connectors. Disengagement during launch is prevented by a cover which spans the board's free edge.

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FAILURE MODE AND CAUSE	FAILURE EFFECT ON END ITEM	RATIONALE FOR ACCEPTANCE
Loss of odd-field sync signal. Cause: (1) Timing Logic, Logic Board. A3, 2294891-502 or 2592392-501	Loss of video routing capability. Worst Case: Loss of mission critical observations via CCTV system.	QUALIFICATION TEST For Qualification Test Flow, see Table 2 located at the front of this book. ACCEPTANCE TEST The CCTV systems' VSU is subjected to the following testing: • Vibration: 20-80Hz: 3 dB/Oct-rise from 0.01 G^2/Hz to 0.04 G^2/Hz 80-350 Hz: 0.04 G^2/Hz 350-750 Hz: 3 dB/Oct-Fall to 0.018 G^2/Hz 750-1000: 0.018 G^2/Hz 1000-2000: 3 dB/Oct-Fall to 0.009 G^2/Hz Test Duration: 1 Minute per Axis Test Level: 6.6 Grms • Thermal: 100° F: Time to stablize equipment plus 1 hour 0° F: Time to stablize equipment plus 1 hour 100° F: Time to stablize equipment plus 1 hour For Acceptance Test Flow, see Table 1 located at the front of this book. OPERATIONAL TEST In order to verify that CCTV components are operational, a test must verify the health of all the command related components from the PHS (A7A1) panel switch, through the RCU, through the sync lines to the Camera/PTU, to the Camera/PTU command decoder. The test must also verify the camera's ability to produce video, the VSU's ability to route video, and the monitor's ability to display video. A similar test would be performed to verify the MDM command path. Pre-Launch on Orbiter Test/In-Flight Test 1. Power CCTV System. 2. Via the PHS panel, select a monitor as destination and the camera under test as source. 3. Send "Camera Power On" command from PHS panel. 4. Select "External Sync" on monitor. 5. Observe video displayed on monitor. Note that if video on monitor is synchronized (i.e., stable raster) then this indicates that the camera is receiving composite sync from the RCU and that the camera is producing synchronized video. 6. Send Pan, Tilt, Focus, Zoom, DLR, AND Gamma commands and visually (either via the monitor or direct observation) verify operation. 7. Select downlink as destination and camera under test as source. 8. Observe video routed to downlink. 9. Send "Camera Power Off" command via PHS panel. 10. Repeat Steps 3 through 9 except issue commands via the MDM command path. This proves that the CCTV equipment is operational.

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SHEET 4 OF 7

FAILURE MODE AND CAUSE	FAILURE EFFECT ON END ITEM	RATIONALE FOR ACCEPTANCE
Loss of odd-field sync signal. Cause: (1) Timing Logic, Logic Board. A3, 2294891-502 or 2592392-501	Loss of video routing capability. Worst Case: Loss of mission critical observations via CCTV system.	QA/INSPECTION Procurement Control - The VSU Parts and hardware items are procured from approved vendors and suppliers, which meet the requirements set forth in the CCTV contract and Quality Plan Work Statement (WS-2593176). Resident DCAS personnel review all procurement documents to establish the need for GSI on selected parts (PAI 517). Incoming Inspection and Storage - Incoming Quality inspections are made on all received materials and parts. Results are recorded by lot and retained in file by drawing and control numbers for future reference and traceability. All EEE parts are subjected to incoming acceptance tests as called for in PAI 315 - Incoming Inspection Test Instructions. Incoming flight parts are further processed in accordance with RCA 1046684 - Preconditioning and Acceptance Requirements for Electronic Parts, with the exception the DPA and PIND testing is not performed. Mechanical items are inspected per PAI 316 - Incoming Inspection Instructions for mechanical items, PAI 305 - Incoming Quality Control Inspection Instructions, and PAI 612 - Procedure for Processing Incoming or Purchased Parts Designated for Flight Use. Accepted items are delivered to Material Controlled Stores and retained under specified conditions until fabrication is required. Non-conforming materials are held for Material Review Board (MRB) disposition. (PAI-307, PAI IQC-531). Board Assembly & Test - Prior to the start of VSU board assembly, all items are verified to be correct by stock room personnel, as the items are accumulated to form a kit. The items are verified again by the operator who assembles the kit by checking against the as-built-parts-list (ABPL). DCAS Mandatory Inspection Points are designated for all printed circuit, wire wrap and welded wire boards, plus harness connectors for soldering wiring, crimping, solder splices and quality workmanship prior to coating of the component side of boards and sleeving of harnesses. Specific VSU board assembly and test instructions are provided in drawing notes, and applicable documents are called out in the fabrication Procedure and Record (FPR-2294823) and parts list PL 2294823. These include wire connection list 2295906, Process Standard RTV-566 2280681, Process Standard - Bonding Velcro Tape 2280809, Specification Soldering 2280749, Specification Name Plate Application 1960167, Specification - Crimping 2280800, Specification - Bonding and Staking 2280878, Specification - Urethane coating 2280877, Specification - locking compound 2026116, Specification Expoxy Adhesive 2010985, Specification - Marking 2280876, Specification - Workmanship 8030035, Specification Bonding and Staking 2280875.

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Loss of add-field sync signal. Cause: (1) Timing logic, Logic Board. A3, 2294891-502 or 2592392-501	Loss of video routing capability. Worst Case: Loss of mission critical observations via CCTV system.	QA/INSPECTION (Continued) VSU Assembly and Test An open box test is performed per TP-IT-22944832, and an Acceptance Test per TP-AT-2294823, including vibration and thermal vacuum. Torques are specified and witnessed, traceability numbers are recorded and calibrated tools are check prior to use. RCA quality and DCAS inspections are performed at the completion of specified FMR operations in accordance with PAI-204, PAI-205, PAI-206, and PAI-217. DCAS personnel witness VSU button-up and critical torquing. RCA and DCAS personnel monitor acceptance tests and review test data/results. These personnel also inspect after all repair, rework and retest. Preparation for Shipment - The VSU is packaged according to 2280746. Process standard for packaging and handling guidelines. All related documentation including assembly drawing, parts list, ADPL, test data, etc. is gathered and held in a documentation folder assigned specifically to each assembly. This folder is retained for reference. An EIDP is prepared for each VSU in accordance with the requirements of MS-2593176. RCA QC and DCAS personnel witness crating, packaging, packing and marking, and review the EIDP for completeness and accuracy.

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FAILURE MODE AND CAUSE	FAILURE EFFECT ON END ITEM	RATIONALE FOR ACCEPTANCE
Loss of odd-field sync signal. Cause: (1) Timing Logic, Logic Board, A3, 2294891-502 or 2592392-501	Loss of video routing capability. Worst Case: Loss of mission critical observations via CCTV system.	FAILURE HISTORY NONE.

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FAILURE MODE AND CAUSE	FAILURE EFFECT ON END ITEM	RATIONALE FOR ACCEPTANCE
Loss of odd-field sync signal. Cause: (1) Timing Logic, Logic Board, A3, 2294091-502 or 2592392-501	Loss of video routing capability. Worst Case: Loss of mission critical observations via CCTV system.	OPERATIONAL EFFECTS Loss of video. Possible loss of major mission objectives due to loss of RMS cameras or other required cameras. CREW ACTIONS If possible, continue RMS operations using alternative visual cues. CREW TRAINING Crew should be trained to use possible alternatives to CCTV. MISSION CONSTRAINT Where possible, procedures should be designed so they can be accomplished without CCTV.