

FMEA NO. <u>2.3.3.1</u> CRITICALITY <u>2/2</u>	SHUTTLE CCTV CRITICAL ITEMS LIST	UNIT <u>TVC/MLA</u> DWG NO. <u>2294819-506, 508/</u> <u>2307088-503</u> SHEET <u>1</u> OF <u>9</u>
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FAILURE MODE AND CAUSE	FAILURE EFFECT ON END ITEM	RATIONALE FOR ACCEPTANCE
<p>Time base errors (jitter) in the synchronization information on the video output line. Video information is present and contains the time base errors.</p> <p><u>IVC</u></p> <p><u>11</u> Sync Generator. Clock Divider Chain. Phase-Locked Loop. 2294880-504</p> <p><u>12</u> Camera Timing Logic 2294881-501</p> <p><u>13</u> Master Oscillator</p> <p><u>IVC</u> Leakers</p>	<p>(1) Loss of camera output depicting scene information within FOV of lens assembly.</p> <p>(2) Loss of camera until self-heating of circuitry restores normal operation.</p> <p><u>Worst Case:</u> Loss of mission critical video.</p>	<p><u>DESIGN FEATURES</u></p> <p>The TVC/Lens Assembly is comprised of 16 electrical subassemblies; 13 subassemblies are RCA Astro designed and fabricated using standard printed-circuit board type of construction. The remaining three assemblies, high voltage power supply, oscillator, and stepper motors, are vendor supplied components which have been specified and purchased according to RCA Specification Control Drawings (SCDs) prepared by engineering and reliability assurance. Specifications per the SCD are prepared to establish the design, performance, test, qualification, and acceptance requirements for a procured piece of equipment.</p> <p>Parts, materials, processes, and design guidelines for the Shuttle CCTV program are specified in accordance with RCA 2295503. This document defines the program requirements for selection and control of EEE parts. To the maximum extent, and consistent with availability, all parts have been selected from military specifications at the JAN level, as a minimum. In addition to the overall selection criteria, a subset of general purpose preferred parts has been defined by this document and the RCA Government Systems Division Standard Parts List. In the case of the CMOS and TTL family of microcircuits, devices are screened and tested to the MIL-STD-883C equivalent and procured under the designations of MI-REL/3HQ and SMC 54LS from RCA-SSD and Texas Instruments Corp, respectively. Parts not included in the above documents have been used in the design only after a nonstandard item approval form (NSIAF) has been prepared, submitted to Reliability Assurance Engineering (RAE) and approved for use in the specific application(s) defined in the NSIAF by NASA-JSC.</p> <p>Worst-Case Circuit Analyses have been performed and documented for all circuit designs to demonstrate that sufficient operating margins exist for all operating conditions. The analysis was worst case-in that the value for each of the variable parameters was set to limits that will drive the output to a maximum (or minimum).</p> <p>A component application review and analysis was conducted to verify that the applied stress on each piece part by the temperature extremes identified with environmental qualification testing does not exceed the stress derating values identified in RCA 2295503.</p> <p>In addition, an objective examination of the design was performed through a POR and COR to verify that the TVC/Lens assembly met specification and contractual requirements.</p>

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FAILURE MODE AND CAUSE	FAILURE EFFECT ON END ITEM	RATIONALE FOR ACCEPTANCE
<p>Time base errors (jitter) in the synchronization information on the video output line. Video information is present and contains the time base errors.</p> <p><u>TYC</u>  <u>A1</u> Sync Generator.          Clock Divider Chain.          Phase-Locked Loop.          2294880-504</p> <p><u>A2</u> Camera Timing Logic          2294881-501</p> <p><u>A13</u> Master Oscillator</p> <p><u>TYC</u>          Heaters</p>	<p>(1) Loss of camera output depicting scene information within FOV of lens assembly.</p> <p>(2) Loss of camera until self-heating of circuitry restores normal operation.</p> <p><u>Worst Case:</u>          Loss of mission critical video.</p>	<p><u>DESIGN FEATURES</u> (Continued)</p> <p><u>BARE BOARD DESIGN</u> (A1)</p> <p>The design of the associated A1 board is constructed from laminated copper-clad epoxy glass sheets (NEMA G-10) Grade FR-4), PER MIL-P-55617A. Circuit connections are made through printed traces which run from point to point on the board surfaces. Every trace terminates at an annular ring. The annular ring surrounds the hole in which a component lead or terminal is located. This ring provides a footing for the solder, ensuring good mechanical and electrical performance. Its size and shape are governed by MIL-P-55640 as are trace widths, spacing and routing. These requirements are reiterated specifically in drawing notes to further assure compliance. Variations between the artwork master and the final product (due to irregularities of the etching process) are also controlled by drawing notes. This prevents making defective boards from good artwork. Holes which house no lead or terminal, but serve only to electrically interconnect the different board layers, contain stitch bars for mechanical support and increased reliability.</p> <p>The thru holes are drilled from a drill tape thus eliminating the possibility of human error and allowing tight control over hole and annular ring concentricity, an important reliability criterion. After drilling and etching, All copper cladding is tin-lead plated per MIL-STD-1495. This provides for easy and reliable soldering at the time of board assembly, even after periods of prolonged storage.</p> <p><u>BOARD ASSEMBLY DESIGN</u> (A1)</p> <p>All components are installed in a manner which assures maximum reliability. Component leads are pre-tinned, allowing total wetting of solder joints. All leads are formed to provide stress relief and the bodies of large components are staked. Special mounting and handling instructions are included in each drawing required after final assembly. The board is coated with urethane which protects against humidity and contamination.</p> <p><u>BOARD PLACEMENT</u></p> <p>The A1 and A3 boards are secured in the electronics assembly by gold-plated beryllium copper card guides. Connections are made to the mother board with blind-mated connectors. Disengagement during launch is prevented by a cover which spans the board's free edge.</p>

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FAILURE MODE AND CAUSE	FAILURE EFFECT ON END ITEM	RATIONALE FOR ACCEPTANCE	
time base errors (jitter) in the synchronization information on the video output line. Video information is present and contains the time base errors.  1 Sync Generator, Clock Divider Chain, Phase-Locked Loop, 2294880-504 2 Camera Timing Logic 2294881-501 3 Master Oscillator  4 Drivers	(1) Loss of camera output depicting scene information within FOV of lens assembly. (2) Loss of camera until self-heating of circuitry restores normal operation.  Worst Case: Loss of mission critical video.	DESIGN FEATURES (Continued)  BARE BOARD CONSTRUCTION (A2)  The A2 board is of "welded wire" construction. At the bare board level this does not distinguish it from a normal PC board except that holes which will take weld pins generally are not connected to PC traces. Only those pins which bring power and ground potentials to the ICs are on PCs. An annular ring surrounds the hole in the board where each power and ground pin is located. These pins are then soldered to the trace like any other component lead. Aside from this feature, all design & construction techniques used in PC board layout apply.  BOARD ASSEMBLY (A2)  The drilled and etched boards are populated with several hundred solderable or weldable pins. Power and ground pins, as well as connector pins, are soldered in place. Discreet components (resistors, diodes, capacitors) are attached to bifurcated terminals, where they are soldered. Flatpack ICs are welded, lead-by-lead, to the tops of the weld pins. After welding, extra lead material is trimmed away. Circuit connections are made using #30 AWG nickel weld wire. The wire is welded to the pin surfaces on the board backside. All wire welds are done using a machine which is tape driven, thus eliminating the possibility of miswiring due to operator error. All wiring & circuit performance is tested prior to box-level installation. After successful testing, components are staked as required by drawing notes and the assembly is coated with urethane.  The board is inserted in the box on card-edge guides, in the same manner as the other PC boards.  The A13 assembly is a temperature compensated voltage controlled crystal oscillator (TCVXO) that is purchased to a specification controlled drawing that establishes the requirements for performance, design, test, and qualification of the unit. The product assurance provisions of the document contain the identical requirements for electronic parts and materials as the Shuttle CCTV program and must receive the approval of RCA and NASA-JSC. Mechanical and electrical integrity of the assembly is confirmed by both analysis (design reviews) and test (qualification and acceptance).	

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FAILURE MODE AND CAUSE	FAILURE EFFECT ON END ITEM	RATIONALE FOR ACCEPTANCE
<p>Time base errors (jitter) in the synchronization information on the video output line. Video information is present and contains the time base errors.</p> <p>YC                      1 Sync Generator.                      Clock Divider Chain.                      Phase-Locked Loop.                      2294880-504                      2 Camera Timing Logic                      2294881-501                      13 Master Oscillator</p> <p>YC                      leaters</p>	<p>(1) Loss of camera output depicting scene information within FOV of lens assembly.                      (2) Loss of camera until self-heating of circuitry restores normal operation.</p> <p><u>Worst Case:</u>                      Loss of mission critical video.</p>	<p><u>QUALIFICATION TEST</u></p> <p>For Qualification Test Flow, see Table 2 located at the front of this book.</p>

FMEA NO. <u>2.3.3.1</u> CRITICALITY <u>2/2</u>	SHUTTLE CCTV CRITICAL ITEMS LIST	UNIT <u>TVC/WLA</u> DWG NO. <u>2294819-506, 508/</u> <u>2307008-503</u> SHEET <u>5</u> OF <u>9</u>																
FAILURE MODE AND CAUSE	FAILURE EFFECT ON END ITEM	RATIONALE FOR ACCEPTANCE																
<p>Time base errors (jitter) in the synchronization information on the video output line. Video information is present and contains the time base errors.</p> <p><u>TVC</u> A1 Sync Generator, Clock Divider Chain, Phase-Locked Loop, 2294880-504</p> <p>A2 Camera Timing Logic 2294881-501</p> <p>A13 Master Oscillator</p> <p><u>TVC</u> Heaters</p>	<p>(1) Loss of camera output depicting scene information within FOV of lens assembly.</p> <p>(2) Loss of camera until self-heating of circuitry restores normal operation.</p> <p><u>Worst Case:</u> Loss of mission critical video.</p>	<p><u>ACCEPTANCE TEST</u></p> <p>The CCTV systems' WLA is subjected directly, without vibration isolators which might be used in their normal installation, to the following testing:</p> <ul style="list-style-type: none"> <li>• Vibration:             <table border="0" style="margin-left: 20px;"> <tr> <td>20-80Hz:</td> <td>3 dB/Oct-rise from 0.01 G<sup>2</sup>/Hz</td> </tr> <tr> <td>80-350 Hz:</td> <td>0.04 G<sup>2</sup>/Hz</td> </tr> <tr> <td>350-750 Hz:</td> <td>-3 dB/10 Oct-slope</td> </tr> <tr> <td>Test Duration:</td> <td>1 Minute per Axis</td> </tr> <tr> <td>Test Level:</td> <td>6.1 Gms</td> </tr> </table> </li> <li>• Thermal Vacuum: In a pressure of 1X10<sup>-5</sup> Torr, the temperature shall be as follows:             <table border="0" style="margin-left: 20px;"> <tr> <td>125° F:</td> <td>Time to stabilize equipment plus 1 hour</td> </tr> <tr> <td>25° F:</td> <td>Time to stabilize equipment plus 1 hour</td> </tr> <tr> <td>125° F:</td> <td>Time to stabilize equipment plus 1 hour</td> </tr> </table> </li> </ul> <p>The WLA may not have been subjected to the vacuum condition.</p> <p>For Acceptance Test Flow, See Table 1 located at the front of this book.</p> <p><u>OPERATIONAL TESTS</u></p> <p>In order to verify that CCTV components are operational, a test must verify the health of all the command related components from the PHS (A7A1) panel switch, through the RCU, through the sync lines to the Camera/PTU, to the Camera/PTU command decoder. The test must also verify the camera's ability to produce video, the VSU's ability to route video, and the monitor's ability to display video. A similar test would be performed to verify the MDM command path.</p> <p><u>Pre-launch on Orbiter Test/In-Flight Test</u></p> <ol style="list-style-type: none"> <li>1. Power CCTV System.</li> <li>2. Via the PHS panel, select a monitor as destination and the camera under test as source.</li> <li>3. Send "Camera Power On" command from PHS panel.</li> <li>4. Select "External Sync" on monitor.</li> <li>5. Observe video displayed on monitor. Note that if video on monitor is synchronized (i.e., stable raster) then this indicates that the camera is receiving composite sync from the RCU and that the camera is producing synchronized video.</li> <li>6. Send Pan, Tilt, Focus, Zoom, OLR, AND Gamma commands and visually (either via the monitor or direct observation) verify operation.</li> <li>7. Select downlink as destination and camera under test as source.</li> <li>8. Observe video routed to downlink.</li> <li>9. Send "Camera Power Off" command via PHS panel.</li> <li>10. Repeat Steps 3 through 9 except issue commands via the MDM command path. This proves that the CCTV equipment is operational.</li> </ol>	20-80Hz:	3 dB/Oct-rise from 0.01 G <sup>2</sup> /Hz	80-350 Hz:	0.04 G <sup>2</sup> /Hz	350-750 Hz:	-3 dB/10 Oct-slope	Test Duration:	1 Minute per Axis	Test Level:	6.1 Gms	125° F:	Time to stabilize equipment plus 1 hour	25° F:	Time to stabilize equipment plus 1 hour	125° F:	Time to stabilize equipment plus 1 hour
20-80Hz:	3 dB/Oct-rise from 0.01 G <sup>2</sup> /Hz																	
80-350 Hz:	0.04 G <sup>2</sup> /Hz																	
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FAILURE MODE AND CAUSE	FAILURE EFFECT ON END ITEM	RATIONALE FOR ACCEPTANCE
<p>Time base errors (jitter) in the synchronization information on the video output line. Video information is present and contains the time base errors.</p> <p><b>VC</b></p> <p>1 Sync Generator. Clock Divider Chain. Phase-locked loop. 2294880-504</p> <p>2 Camera Timing Logic 2294881-501</p> <p>13 Master Oscillator</p> <p><b>VC</b> Drivers</p>	<p>(1) Loss of camera output depicting scene information within FOV of lens assembly.</p> <p>(2) Loss of camera until self-heating of circuitry restores normal operation.</p> <p><b>Worst Case:</b> Loss of mission critical video.</p>	<p><b>QA INSPECTION</b></p> <p><b>Procurement Control</b> - The TVC/MLA EEE Parts and hardware items are procured from approved vendors and suppliers, which meet the requirements set forth in the CCTV contract and Quality Plan Work Statement (WS-2593176). Resident OCAS personnel review all procurement documents to establish the need for GSI on selected parts (PAI 517).</p> <p><b>Incoming Inspection and Storage</b> - Incoming Quality inspections are made on all received materials and parts. Results are recorded by lot and retained in file by drawing and control numbers for future reference and traceability. All EEE parts are subjected to incoming acceptance tests as called for in PAI 315 - Incoming Inspection Test Instructions. Incoming flight parts are further processed in accordance with RCA 1846684 - Preconditioning and Acceptance Requirements for Electronic Parts, with the exception that DPA and PIND testing is not performed. Mechanical items are inspected per PAI 316 - Incoming Inspection Instructions for mechanical items, PAI 305 - Incoming Quality Control Inspection Instruction, and PAI 612 - Procedure for Processing Incoming or Purchased Parts Designated for Flight Use. Accepted items are delivered to Material Controlled Stores and retained under specified conditions until fabrication is required. Non-conforming materials are held for Material Review Board (MRB) disposition. (PAI 307, PAI IQC 531).</p> <p><b>Board Assembly &amp; Test</b> - Prior to the start of TVC board assembly, all items are verified to be correct by stock room personnel, as the items are accumulated to form a kit. The items are verified again by the operator who assembles the kit by checking against the as-built-parts-list (ABPL). OCAS Mandatory Inspection Points are designated for all printed circuit, wire wrap and welded wire boards, plus harness connectors for soldering wiring, crimping, solder splices and quality workmanship prior to coating of the component side of boards and sleeving of harnesses.</p> <p style="text-align: center;"><b>TVC Boards</b></p> <p>Specific TVC board assembly and test instructions are provided in drawing notes, and applicable documents are called out in the Fabrication Procedure and Record (FPR-2294819) and parts list PL2294819. These include shuttle TVC assembly notes 2593660, Process Standard RTV-566 2280881, Process Standard - Bonding Velcro Tape 2280889, Specification Soldering 2280749, Specification Name Plate Application 1960167, Specification - Crimping 2280800, Specification - Bonding and Staking 2280878, Specification - Urethane coating 2280877, Specification - Locking compound 2026116, Specification Epoxy Adhesive 2010985, Specification - Marking 2280875, Specification - Workmanship 8030035, Specification Bonding and Staking 2280875.</p>

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FAILURE MODE AND CAUSE	FAILURE EFFECT ON END ITEM	RATIONALE FOR ACCEPTANCE
<p>Time base errors (jitter) in the synchronization information on the video output line. Video information is present and contains the time base errors.</p> <p><u>IVC</u></p> <p><u>A1</u> Sync Generator, Clock Divider Chain, Phase-Locked Loop, 2294800-504</p> <p><u>A2</u> Camera Timing Logic 2294801-501</p> <p><u>A13</u> Master Oscillator</p> <p><u>IVC</u> Heaters</p>	<p>(1) Loss of camera output depicting scene information within FOV of lens assembly.</p> <p>(2) Loss of camera until self-heating of circuitry restores normal operation.</p> <p><u>Worst Case:</u> Loss of mission critical video.</p>	<p><u>QA INSPECTION (Continued)</u></p> <p><u>IVC Assembly and Test</u> - An open box test is performed per TP-IT-2294819, and an Acceptance Test per TP-AT-2294819, including vibration and thermal vacuum. Torques are specified and witnessed, traceability numbers are recorded and calibrated tools are checked prior to use. RCA Quality and DCAS inspections are performed at the completion of specified FPR operations in accordance with PAI 204, PAI 205, PAI 206 and PAI 217. DCAS personnel witness TVC button-up and critical torquing.</p> <p><u>WLA Assembly and Test</u> - An open box test is performed per TP-IT-2307008, Acceptance Test per TP-AT-2307008. Torques are specified and witnessed, traceability numbers are recorded and calibrated tools are checked prior to use. RCA Quality and DCAS inspections are performed at the completion of specified FPR operations in accordance with PAI 204, PAI 205, PAI 217 and PAI 402. DCAS personnel witness WLA button-up and critical torquing.</p> <p><u>IVC/WLA Assembly and Test</u> - After a TVC and a WLA have been tested individually, they are mated and a final acceptance test is performed per TP-AT-2294819, including vibration and thermal vacuum environments. RCA and DCAS personnel monitor these tests and review the acceptance test data/results. These personnel also inspect for conformance after all repair, rework and retest.</p> <p><u>Preparation for Shipment</u> - The TVC and WLA are separated prior to shipment after fabrication and testing is complete. Each is packaged according to CCTV Letter 8011 and 2280746, Process standard for Packaging and Handling guidelines. All related documentation including assembly drawings, Parts List, ABPL, Test Data, etc., is gathered and held in a documentation folder assigned specifically to each assembly. This folder is retained for reference. An EIDP is prepared for each assy in accordance with the requirements of MS-2593176. RCA QC and DCAS personnel witness crating, packaging, packing and marking, and review the EIDP for completeness and accuracy.</p>

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<p>time base errors (jitter) in the synchronization information on the video output line. Video information is present and contains the time base errors.</p> <p><u>VC</u>                  1 Sync Generator.                  Clock Divider Chain.                  Phase-Locked Loop.                  2294880-504</p> <p>2 Camera Timing Logic                  2294881-501</p> <p>13 Master Oscillator</p> <p><u>VC</u>                  leaters</p>	<p>(1) Loss of camera output depicting scene information within FOV of lens assembly.</p> <p>(2) Loss of camera until self-healing of circuitry restores normal operation.</p> <p><u>Worst Case:</u>                  Loss of mission critical video.</p>	<p><u>FAILURE HISTORY</u>                  NONE.</p>



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<p>time base errors (jitter) in the synchronization information on the video output line. Video information is present and contains the time base errors.</p> <p><u>VC</u></p> <p>1 Sync Generator. Clock Divider Chain. Phase-Locked Loop. 2294880-504</p> <p>2 Camera Timing Logic 2294881-501</p> <p>13 Master Oscillator</p> <p><u>VC</u> operators</p>	<p>(1) Loss of camera output depicting scene information within FOV of lens assembly.</p> <p>(2) Loss of camera until self-heating of circuitry restores normal operation.</p> <p><u>Worst Case:</u> Loss of mission critical video.</p>	<p><u>OPERATIONAL EFFECTS</u></p> <p>Loss of video. Possible loss of major mission objectives due to loss of RMS cameras or other required cameras.</p> <p><u>CREW ACTIONS</u></p> <p>If possible, continue RMS operations using alternative visual cues.</p> <p><u>CREW TRAINING</u></p> <p>Crew should be trained to use possible alternatives to CCTV.</p> <p><u>MISSION CONSTRAINT</u></p> <p>Where possible, procedures should be designed so they can be accomplished without CCTV.</p>