Part Number(s): 000566-01

	Name	Part Number(s)	Qty	Sheet No.	Schematic No.
Item:	Host Processor CCA	000801-02	1		
	Video Input CCA	000574-03	1		000625
	Video Output CCA	000575-02	1		000628
	Video Processor CCA	000576-02	1		000630

Function: Video Input CCA

On the VIC, the two video signals conditioned by the VSC are fed to two NTSC decoder devices where the colour signal is filtered out and the videos are digitized by Analog to Digital converters. The digitized video is stored in two 1024 x 512 x 16 Video Random Access Memory (VRAM) banks for 8 bit digitized video processing on this card, and is also routed to the VPC. The 40MHz TMS320C40 Digital Signal Processor (DSP^2) on this card provides the Video Input Processor (VIP) function. The DSP has 128K x 32 Static RAM (SRAM) for code and data storage. The SRAM has Error Detection and Correction (EDAC) which provides the capability for single bit error correction and multiple bit error detection. The VIP receives window position and threshold parameters from the HPC via the Host VME Bus interface through a 4K x 16 dual port memory. The VIP uses this data to process the digitized video from the VRAM and to generate a threshold map which is stored in the DSP RAM and passed to the VPC using a C40 communication port connection.

Video Output CCA

The VOC card provides the Video Output Processor (VOP) function, which is essentially a graphics accelerator. This card contains two Double buffered VRAMs of 768 pixels x 480 lines controlled by a 40MHz TMS320C40 DSP located on this card. The DSP has EDAC protected SRAM and a dual port RAM for communication with the HPC via the VME Bus interface, of similar design to the DSP located on the VIC. The VOP receives graphic primitives and enhancement overlay controls from the HPC via the Host VME Bus interface. This DSP then generates and stores in memory the graphics for each of the video outputs. Two RGB to NTSC encoders provide two separate video outputs which are independently phase locked to either Camera 1 or 2 and can be used for Graphical User Interface (GUI), Synthetics or video enhancements. Each encoder can generate 4 colour text and 16 colour graphics. A software controlled video look-up table translates 4/16 colours to any 24 bit colour. The VOP also stores data in the VRAMs to control selection of the enhancement overlays. The NTSC video outputs and overlay control bits are fed to the multiplexers on the VBC.

Video Processor CCA

The VPC provides the Image Pre-Processor (IPP) function for the two Video Input channels. The two digital video channels and the threshold from the VIC are fed to two custom hardware video processing channels, implemented in an ACTEL 1020 FPGA, which generate the binary video signal and the accumulated line moment and area for each channel. The binary video generated on this card is routed to the VBC for video output. The accumulated line areas, moments and binary video are stored in 4K x 32 DPRAMs accessible by a 40MHz TMS320C40 DSP located on this card. The DPRAMs buffer two lines of video data. The DSP accumulates window X and Y moments and calculates centroids. The DSP has EDAC protected SRAM and a dual port RAM for communication with the PPC via the VME Bus interface, of similar design to the DSP located on the VIC.

Host Processor CCA

The HPC is a COTS PC compatible ruggedized Industry Standard Extended VME Bus (64 bit) card based on the 133MHz Intel Pentium Processor. The HPC uses a COTS Basic I/O Subsystem (BIOS), Real Time Clock with battery backup power and includes 16M EDO RAM with EDAC protection and 256K cache. Peripheral drivers include the RS-422 serial interfaces to connect to the Orbiter PGSC, a VGA video driver, keyboard / trackball PS2 interfaces, and an enhanced IDE Hard drive. The HPC interfaces to the VIC, VPC, VOC and IFC via the VME Bus and provides photogrammetric solutions, coordinate system transformations, synthetic and enhanced display generation, camera control, single joint operations and calibration data.

Failure Mode: EDAC protected memory single bit error

	H/W	Func.	Screen Failures
Criticality:	3	1F	

Mission Phase: Orbit

Cause(s):	Host Processor CCA	EDAC Protected DRAM Single bit hard error
		EDAC Protected DRAM Single bit soft error
	Video Input CCA	VIC DSP SRAM Single Bit Hard Error
		VIC DSP SRAM Single Bit Soft Error
	Video Output CCA	VOC DSP SRAM Single Bit Hard Error
		VOC DSP SRAM Single Bit Soft Error
	Video Processor CCA	VPC C40 SRAM Memory Single Bit Hard Error
		VPC C40 SRAM Memory Single Bit Soft Error

Failure effect on unit/end item: 1. OSVU: No effect. The EDAC circuitry is detecting and correcting the error immediately. For additional bit errors in the affected memory location, EDAC will no longer be able to correct the error until the error is corrected by background scrubbing (update rate - 20 minutes) used to prevent accumulation of errors. In the case of a hard single bit failure, background scrubbing will be ineffective.
2. Interfacing Subsystems: No effect.
3. Mission: No effect.
4. Crew/Vehicle: No effect until subsequent failure of the EDAC circuitry such that it is no longer correcting memory errors which may result in the display of erroneous data to the operator.
5. Operational Considerations: The Crew is trained to use as many cues as possible to perform any mating/berthing task and insure the cues are consistent with pre-flight training. The available cues to perform mating/berthing tasks include the OSVU steering display, RMS digitals, out the window views, other camera views, and EVA personnel as necessary. To prevent the crew from using corrupted data, the graphical cue (i.e. Steering Display) provided by the OSVU will not be the only cue used to perform a mating/berthing task. If the cues are inconsistent, the operation will be paused, and the crew will check MCC for futher evaluation.

Worst Case: No effect until subsequent failure

Redundant Paths: EDAC detects and corrects single bit memory errors immediately
The Crew is trained to use as many cues as possible to perform any mating/berthing task and insure the cues are consistent with pre-flight training. The available cues to perform mating/berthing tasks include the OSVU steering display, RMS digitals, out the window views, other camera views, and EVA personnel as necessary. To prevent the crew from using corrupted data, the graphical cue (i.e. Steering Display) provided by the OSVU will not be the only cue used to perform a mating/berthing task. If the cues are inconsistent, the operation will be paused, and the crew will check MCC for futher evaluation.

Failure Detection: None
Operator detects corrupt OSVU data by verifying consistency of OSVU Steering Display cues with redundant operator cues (RMS digitals, out the window views, other camera views, and EVA personnel)

Corrective Action: EDAC detects and corrects single bit memory errors immediately

Time to Effect: Immediate

Time to Correct: Immediate

Hazard/Remarks: As a design this failure mode is a 2/1R criticality because the EDAC circuit acts as a redundant path for an EDAC protected single bit error. Given the scenario outlined below there is a possibility that incorrect data could be presented to the operator which without the use of alternate operator cues might result in damage to the Crew/Vehicle if the EDAC circuit fails between the time a single bit error occurs and the data item is accessed. However this failure mode criticality has been reduced to an operationnal criticality of 3/1R through the crew use of alternate operator cues. The following sequence of events outlines the scenario.

1. A bit is flipped within a static parameter (constant, lookup table, database item) or executable instruction.

2. The EDAC circuitry fails in such a way that this corrupted data is passed through without being corrected.

3. This corrupted static data causes an error in the displayed photo-solution.

4. This error does not cause any of the error limits to be exceeded or otherwise trigger a software or unrecoverable error.

5. The Crew is trained to use as many cues as possible to perform any mating/berthing task and insure the cues are consistent with pre-flight training. The available cues to perform mating/berthing tasks include the OSVU steering display, RMS digitals, out the window views, other camera views, and EVA personnel as necessary. To prevent the crew from using corrupted data, the graphical cue (i.e Steering Display) provided by the OSVU will not be the only cue used to perform a mating/berthing task. If the cues are inconsistent, the operation will be paused, and the crew will check MCC for futher evaluation.

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Rev 1 of FMEA 27 Oct 1998: Changes made as a result of subsequent review with NASA MOD and indication that other redundant cues were available to verify OSVU cues.

Changed criticality: Changed From 2/1R To 3/1R
Changed Effect:
Changed Item 4 to delete reference to collision
Added Item 5: Operational Considerations: ...
Changed Detection:
Added Item 2 "Operator detects corrupt OSVU data by verifying.... consistency of OSVU Steering Display cues with redundant operator cues (RMS digitals, out the window views, other camera views, and EVA personnel
Changed Redundant Path:
Added item 2 "The Crew is trained to use as many cues as possible... If the cues are inconsistent...the crew will check MCC for futher evaluation."
Remarks:
Changed first para to indicate design is crit 2/1R but use of redundant cues reduces criticality to 3/1R
Changed item 5 in remarks to refer to redundant cues

Approvals:

Functional Group	Name	Position	Telephone	Date Signed	Status
Engineer	Brule, Dave / Neptec	Design Engineer	613-599-7602 EX	02Nov98	Signed
Reliability	Elgin, David / Neptec	QA Engineer	613-599-7603X2	02Nov98	Signed
Program Management Offi	Beach, Larisa / Neptec	SVS Program Manager	613 599 7602 EX	04Nov98	Signed
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